

# Advantages of Field Programmable Gate Arrays



FPGAs - Field Programmable Gate Arrays - are future-oriented building bricks which allow perfect customization of the hardware at an attractive price even in low quantities. FPGA components available today have usable sizes at an acceptable price. This makes them effective factors for cost savings and time-to-market when making individual configurations of standard products. A time consuming and expensive redesign of a board can often be avoided through application-specific integration of IP cores in the FPGA - an alternative for the future, especially for very specialized applications with only small or medium volumes.

And that's not all. FPGA technology is indispensable wherever long-term availability or harsh industrial environments are involved. IP cores per se are not threatened by discontinuation, even if an FPGA component may be replaced by a newer one after 10 years, for instance. In addition, the Cyclone devices from Altera are qualified for an operation temperature of -40 to +85°C right from the start.

## Harsh Environments

One of the most critical requirements is a qualified operational temperature between -40 and +85°C. Many parts however can only be screened because the component manufacturer often does not guarantee the needed temperature range. Since the functionality of many of these components can now be programmed in FPGA, there is only one part which must be in accordance with the requirements and this is the FPGA itself. The Altera Cyclone FPGAs are defined for -40 to +85°C operation temperature. As required by standards like the EN 50155 railway norm the FPGA is used only in the specification range of the component data sheet. It conforms to EN, CECC or IEC standards, is manufactured according to ISO 9000 and a second source is also available.

## Long-Term Availability

Another important aspect is long-term availability. Many component manufacturers don't agree on any long-term availability, some guarantee 5 years, and very few go up to 10 years. This makes it difficult or impossible for the board manufacturer to support his product for more than 10 years. A significant example are mainstream graphics controllers which stay on the market for a few months maximum. The advantage of FPGAs and their nearly unlimited availability lies in the fact that — even if the device migrates to the next generation — the code remains unchanged. This is in accordance with norms like the EN 50155 which prescribes that customized parts like FPGAs must be documented to allow reproduction and that the documentation and the source code must be handed out to the customer.

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## Typical I/O Functions in FPGA

MEN uses FPGA technology based on the Altera Cyclone devices on most of its more recent single board computers and on many I/O cards for VMEbus, CompactPCI or stand-alone platforms and on its ESM Embedded System Modules. A part of the FPGA functions may be necessary for the general operability of the board itself. Other functions extend the I/O capabilities of the board. MEN offers a continuously growing pool of IP cores, for example:

- Different graphics controllers, touch
- Field bus interfaces such as CAN bus and MVB
- Various types of UARTs like RS232, RS485...
- Ethernet and HDLC communication
- IDE and floppy controllers
- SRAM and Flash memory controllers
- GPIO, binary I/O, counter, quadrature decoder and PWM functions
- ...and more functions to come and/or on request

All these IP cores can be combined with those available from Altera (Avalon bus) and/or IP cores available from the OpenCores community (Wishbone bus). MEN also supports development around the Nios soft core processor from Altera. A Wishbone-to-Avalon and an Avalon-to-Wishbone bridge developed by MEN allow interoperability between Avalon and Wishbone devices.

## The FPGA Structure

The standard programming language for MEN IP cores is VHDL and the supported standard bus is Wishbone.

As the software views the FPGA as a PCI device, MEN has defined a ROM memory structure that allows recognition of the individual functions and their resources and subsequent driver design.

Loading of the FPGA is done dynamically. After power-on the FPGA is not yet loaded, all pins are tri-state. The CPU BIOS now first loads the FPGA. To do this a part of the BIOS Flash memory is reserved. Common BIOS Flash update mechanisms can flash the memory contents and thus change I/O functionality. And even when the operating system has booted up, the FPGA can be reprogrammed at any time. For instance, you could first load basic functionality through BIOS, e. g. a CAN controller. The operating system can then add the remaining functionality depending on the device configuration—for example a graphics controller or UARTs.

## Develop and integrate your own IP cores or let MEN do it

Every MEN board which allows customization of the application-specific I/O in FPGA comes with a standard factory configuration of IP cores developed by MEN. Implementation of additional and/or different functions depends on the individual pin count of the board and the number of logic elements available in the FPGA. The pin counts and logic elements needed



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by the single IP cores can be learned from our IP core compare chart. Whether you want MEN to do individual core development and FPGA integration or whether you prefer doing it yourself, you have a number of options – see separate description “FPGA Development Services”.



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